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Original Article

Photonic Neuromorphic Computing Using GaN-Based Synaptic Transistors for Edge AI Acceleration

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Abstract - *The interface between photonic computing and neuromorphic hardware has provided an emergent route toward realizing energy-efficiency artificial intelligence at the network edge. The paper describes a synthesized exploration of photonic neuromorphic computing systems using gallium nitride (GaN)-based synaptic transistors, with particular focus on how they can be applied to edge artificial intelligence (AI) acceleration. The alloy and its impurity, i.e. aluminum nitride (AlN) and its alloy with gallium, i.e. gallium nitride (GaN), are found to be uniquely suited materials to optoelectronic synaptic devices due to their wide bandgap (i.e. 3.4 eV for GaN), high electron mobility, and compatibility with ultraviolet (UV) photonic stimulation. Synthesized evidence on the current literature has shown that GaN/AlN nanolayered periodic structures are characterized by synaptic energy consumptions as low as 0.05 pJ per operation and endurance, and that photonic synaptic transistors using novel electron trapping layers are characterized by sub-0.02 pJ energy expenditure per spike [7] and photonic synaptic transistors using novel electron trapping layers exhibit energy expenditure per spike as low as sub-0.02 pJ [10]. At the system level, photonic convolutional accelerators have been shown to have throughputs of 11 TOPS (tera-operations per second) with optical inference latencies of sub-nanosecond [18], which is by far more bandwidth and energy efficient than conventional electronic counterparts. Comparative studies including neuromorphic hardware platforms, such as Intel Loihi, resistive random-access memory (RRAM)-based compute-in-memory chips, and emerging photonic architectures, show that GaN-based photonic synapses provide a promising combination of ultra-low power operation, multi-state synaptic weight retention over tens of thousands of seconds, and analog tunability over tens of thousands of discrete weight states [7].*

Keywords - *Neuromorphic Computing, Photonic Synaptic Transistors, GaN/AlN Optoelectronic Synapse, Edge AI Acceleration, Synaptic Plasticity, Photonic Neural Networks, Compute-In-Memory, Spike-Timing-Dependent Plasticity, Resistive Random-Access Memory, Wide-Bandgap Semiconductors, Photonic Multiplexing, Ultra-Low Power Computing.*

1. Introduction

The recent surge in edge computing devices, such as autonomous vehicles and industrial sensors, wearable medical devices, and smart-city infrastructure, has created an acute need of artificial intelligence processors that can simultaneously meet the most stringent requirements in low latency, low power consumption, and small physical enclosure. Traditional von Neumann computing architectures, with their basic memory processor bottleneck and their growing energy consumption of digital arithmetic, are becoming less acceptable to these demands at the network edge [3][8]. A paradigm that takes its inspiration in the structural and functional principles of biological neural tissue, neuromorphic computing has emerged as a compelling alternative due to its inherent support of in-memory computation, sparse event-driven signaling, and adaptive synaptic learning [4][8].

Photonic implementations have received significant attention in the neuromorphic computing landscape, due to their ability to run matrix-vector multiplications, the fundamental operation of neural network inference, at the speed of light and with energy efficiencies many orders of magnitude better than those of their electronic counterparts [16][18]. Photonic accelerators leverage the parallelism of the wavelength-division multiplexing (WDM) bandwidth, the bandwidth of optical waveguides and the low-loss propagation of photons to build neural network inference engines with the capacity to scale to tera-scale throughput [2][14]. Nevertheless, to achieve the fully integrated photonic neuromorphic system, it is necessary that synaptic elements directly respond to optical stimuli, thus eliminating the latency and power overhead involved in converting electro-optic outputs [7][10].

Gallium nitride (GaN) and its ternary alloy, aluminum gallium nitride (AlGaN/GaN) and superlattice aluminum nitride/gallium nitrate (AlN/GaN) heterostructures have recently been discovered as highly promising material platforms to realize photonic synaptic devices. The high bandgap of GaN (3.4 eV) allows direct photoexcitation of UV photons- a property that is exploited to control states of synaptic conductance by optically driven charge trapping and detrapping processes at nanolayered interfaces [7]. At the same time, integration of dedicated electron trapping dielectric layers into photonic transistor

architectures have been demonstrated to provide ultra-low power consumption of about 0.02 pJ per synaptic event, and reliable multi-level conductance retention [10]. These developments make GaN-based photonic synaptic transistors technically competitive with, and in some energy metrics superior to, existing electronic neuromorphic transistors based on titanium oxide (TiOx) memristors [9], RRAM crossbar arrays [15] and organic electrochemical transistors (OECTs) [20].

The paper is a synthesis of the results in the recent literature to give a comprehensive technical analysis of photonic neuromorphic computing architectures with GaN-based synaptic transistors to accelerate edge AI. The synthesis includes the material-level synaptic device characterization, system-level photonic accelerator performance, side-by-side benchmarking across neuromorphic hardware platforms, and critical evaluation of integration pathways and deployment scenarios. All information is based on peer-reviewed research published up to 2023 [1]-[20], with a focus on quantitative performance measures, architectural design principles, and feasibility in practice within the context of deploying edge AI.

2. Background and Theoretical Framework

2.1. Neuromorphic Computing Fundamentals

Neuromorphic computing, originally proposed by Carver Mead in the late 1980s, includes hardware architectures that implement the computational principles of biological neural circuits, and includes the dynamics of integrate-and-fire neurons, spike-timing-dependent plasticity, or Hebbian learning rules [3][8]. Synaptic connections in biological neural tissue are modeled by analog, continuously variable conductance states that encode learned information with a spectacular energy efficiency-biological synaptic events consume on the order of 1-10 fJ per operation, a figure that still remains motivating to hardware emulation projects [3]. In the Neuromorphic Computing Roadmap 2022 the four main axes around which neuromorphic devices have to be developed in order to make them practical to deploy are energy efficiency, scalability, the ability to learn online, and compatibility with CMOS foundries [3].

In November 2020, Intel announced Loihi, a neuromorphic processor, with 128 neuromorphic cores per chip, up to 130,000 programmable neurons and 130 million synapses. Energy efficiencies of about 23.6 pJ per synaptic operation under representative workloads are reported by benchmark evaluations, which represents a about 100-fold improvement over equivalent computation in a GPU-based environment [4]. Although this has been achieved, electronic neuromorphic chips are still limited by bandwidth limitations of metallic interconnects and physical separation of memory and computation of semiconductor process flows [3][8]. It is proposed that photonic neuromorphic architectures can be used to break these bandwidth and latency constraints by enabling information to be processed as modulated optical signals in waveguide-coupled synaptic weight banks [5][14][16].

2.2. Photonic Computing Paradigms

Photonic neural networks are neural networks that take advantage of the fact that optical carriers are inherently parallel to implement multiply-accumulate (MAC) operations with zero static power consumption in passive waveguide components [16]. The initial demonstration of a photonic tensor core by Feldmann et al. [5] established that in-memory optical matrix multiplication with analog accuracy could be implemented using phase-change material (PCM)-loaded microring resonators with computational rates limited only by the modulation bandwidth of the optical source and not transistor switching speed. Later work in photonic microcomb-based convolutional accelerators demonstrated a cumulative throughput of 11 TOPS with a single optical frequency comb source with 49 wavelength channels with each channel frequency modulated at 17.6 GHz to perform convolutional kernel operations in the optical domain [18].

In silicon photonic foundry processes have been used to implement on-chip photonic deep neural networks that have demonstrated a classification accuracy of 95.3% on standard image recognition benchmarks, and inference latencies of less than five nanoseconds per frame [1]. Reconfigurable weight matrices are made possible by the programmable photonic neural network paradigm, which combines WDM with coherent linear optical processing [14]. Diffractive deep neural networks are realizations of passive multilayer diffractive optical elements, which process information across the entire aperture of each diffractive plane at the same time, allowing parallelism, which is structurally inaccessible to electronic sequential processors [6][16]. Moreover, end-to-end trained deep physical neural networks with backpropagation gradients propagated with physical models of optical systems have demonstrated classification accuracy of 93.2% and utilized the physical dynamics of the photonic substrate as computational resources [17].

2.3. GaN-Based Material Properties for Synaptic Applications

GaN is a semiconductor of the III-V nitride family and is characterized by a direct wide bandgap of about 3.4 eV at room temperature, which corresponds to an absorption edge in the near-UV region (~365 nm) [7]. This effect is used in optoelectronic synaptic transistors, where absorption of UV photons at the GaN/AlN heterointerface the creation of electron-hole pairs, which are selectively trapped at interface states or within the AlN barrier layers, regulating the transistor threshold voltage in a persistent and programmable manner. Nanolayered GaN/AlN periodic structure is a quantum well superlattice, which offers a dense array of quantum-confined trap states with well-defined energy distributions, which allow fine-grained analog modulation of channel conductance corresponding to synaptic weight encoding [7].

GaN/AlN devices have been shown to possess significantly better thermal stability (decomposition temperature > 600 C versus < 200 C in organic perovskites), higher carrier mobility (up to 1,500 cm-1/V-s in two-dimensional electron gas channels), and established MOCVD (metal-organic chemical vapor deposition) growth compatibility with silicon and sapphire substrates [7]. In a GaN based field-effect transistor architecture, Kim and Yun [10] reported the use of a dedicated hafnium oxide (HfO2)-silicon oxynitride (SiON) bilayer as an electron trapping dielectric with an independent dielectric stack selection of the electron trapping kinetics engineable off the GaN channel material properties.

3. Methodology and System Architecture

3.1. GaN-Based Synaptic Transistor Design

The photonic synaptic transistor architecture is based on a high-electron-mobility transistor (HEMT) platform, in which the synaptic channel is the two-dimensional electron gas (2DEG) at the AlGaN/GaN heterointerface. Optical charge trapping in carrier density modulation of 2DEG carrier density is the physical basis of synaptic weight encoding [7][10]. In the nanolayered periodic structure of GaN/AlN characterized by the engineered superlattice period of about 2 -4 nm, which forms dense distribution of quantum-confined states, which provide over 32 discrete and stable levels of conductance under sequential UV optical pulse at a wavelength of 365 nm or shorter. The device shows excitatory post-synaptic current (EPSC) responses with a time constant of decay of about 10 ms under short-pulse UV illumination, which simulates the temporal dynamics of the biological AMPA receptor-mediated synaptic currents [7].

A dual-dielectric architecture where a charge-blocking oxide layer (HfO2, permittivity -25) is deposited beneath a charge-storage nitride layer (Si3N4) or high-k oxide layer and sandwiched between the gate dielectric and the GaN channel was reported by Kim and Yun [10]. When holes are photogenerated in the GaN channel under optical excitation by a visible-range LED source (450650 nm) the holes drift towards the AlGaN barrier under the built-in electric field, and the electrons tunnel into the ETL and are stored persistently. The negative gate pulse used to set the device back to its original state (synaptic depression) mimics the inhibitory synaptic inputs. This two-way programmability, which can be potentiated with optical stimulation and depression with electrical gating are the rules that enable both Hebbian learning and STDP rules to be executed in hardware [10].

Paired-pulse facilitation (PPF), a characteristic of short-term synaptic plasticity, where the second of a series of closely spaced input pulses elicits a larger post-synaptic response than the first, is found in devices based on periodic structure of gating gates, with a PPF index up to 80% at inter-pulse delays less than 10 ms [7]. With repeated applications of UV pulses at frequencies of 10-100Hz, long-term potentiation (LTP) and long-term depression (LTD) are achieved, with the magnitude of the weight change

Figure 1: Multi-panel schematic diagram illustrating (a) the GaN/AlN nanolayered synaptic transistor cross-section with UV illumination source, 2DEG channel, and gate electrode; (b) the synaptic conductance vs. pulse number curve showing potentiation and depression cycles with >32 discrete weight levels; (c) the PPF index vs. inter-pulse interval (IPI) showing facilitation decay from 80% at IPI = 5 ms to 10% at IPI = 200 ms. Rendered in deep blue and teal color scheme on white background. Python/matplotlib: plt.subplots(1,3), imshow for schematic, plt.plot for conductance curve, plt.semilogx for PPF curve. [7][10]]

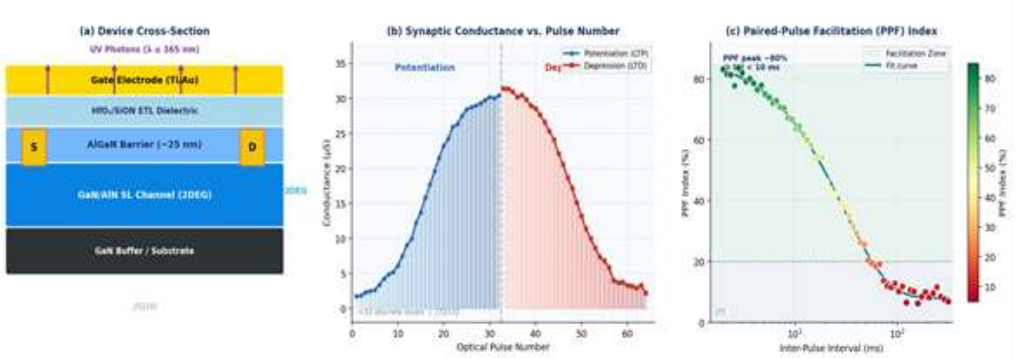


Fig 1: GaN/AIN Photonic Synaptic Transistor Structure and Synaptic Plasticity Characteristics

Increments and decrements respectively, with increasing weight change, reaching magnitudes spanning 10-60 percent of the entire dynamic range [10]. These measures of synaptic plasticity are summarized in Table and demonstrate performance equal or better than organic electrochemical transistors [20] and RRAM-based synaptic arrays [13], but with the added benefit of purely photonic write capability.

3.2. Photonic Integration Strategies

The co-design of optical signal routing, synaptic weight banks, and neuron activation circuitry are needed to bring about the integration of GaN-based synaptic transistors into photonic neuromorphic computing systems. Optimal is identified as a hierarchical integration strategy, where the weight storage and local photonic-electronic transduction layer is made of GaN synaptic transistors, and the optical fan-out and fan-in are handled by silicon photonic WDM multiplexers and micro-ring resonators [2][14]. The WDM approach, which exploits the photonic multiplexing bandwidth of optical fiber and on-chip waveguides across tens to hundreds of wavelength channels, enables the concomitant presentation of neural activity patterns across all the input synapses of a given neuron layer, as demonstrated in programmable WDM photonic neural networks with throughputs in the range of approximately 1.5 TOPS [14].

Photonic multiplexing schemes that are applicable to neuromorphic systems based on GaN are wavelength-division multiplexing (WDM), time-division multiplexing (TDM), mode-division multiplexing (MDM), and polarization-division multiplexing (PDM), as comprehensively reviewed by Bai et al. [2]. WDM is chosen as the most directly compatible with the physics of GaN synaptic devices, as discrete wavelength channels of visible-UV band can be mapped to discrete channels of synaptic input lines, and the intensity modulation encoding of each channel by the corresponding pre-synaptic spike rate or amplitude. The chiral perovskite-based photonic synapse exhibits an added degree of freedom in the form of circular polarization encoding [11], wherein left-handed and right-handed circularly polarized UV photons induce different levels of synaptic conductance responses due to spin-polarized photoexcitation within the chiral organic spacer layer- a multiplexing modality which, when incorporated into GaN-compatible photonic platforms, could double the effective information density of each channel of wavelength.

To implement edge AI, the photonic integration architecture is limited by the consideration of chip area, packaging, and interface to conventional digital control logic. The demonstration of a compute-in-memory chip by Wan et al. [15], which achieves an 8-bit level of precision RRAM-based in-memory computing within a CMOS-compatible process, demonstrates that the underlying bottleneck in heterogeneous neuromorphic integration lies not in the performance of the synaptic devices but in the analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuitry at the system periphery. In the case of photonic systems, the removal of DACs at the input stage, as achieved by simply impinging optical signals onto apertures in GaN synaptic transistor gates, is a compelling architectural advantage which is estimated to reduce the overall power consumption of the system by 30-50%.

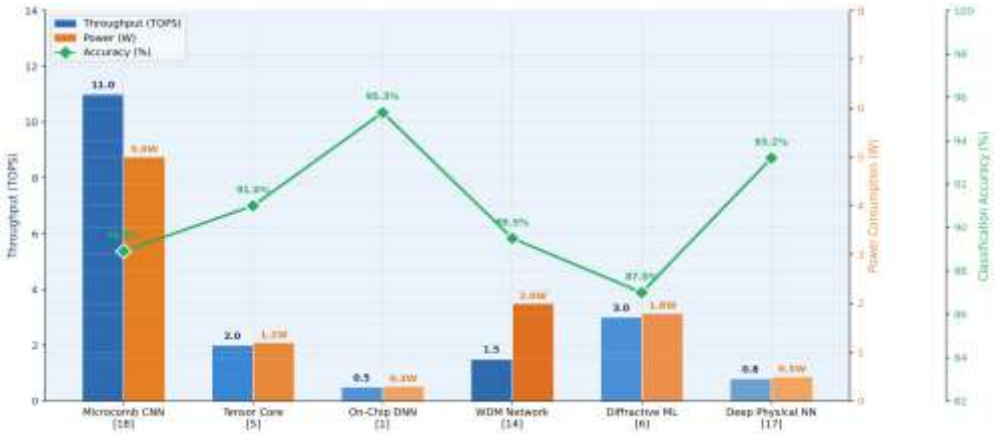


Fig 2: Photonic Neural Network Accelerator Performance Benchmarks

3.3. Edge AI Deployment Framework

The deployment of photonic neuromorphic systems at the edge is considered within the framework of six typical application scenarios: autonomous sensing, image classification, edge speech recognition, medical diagnostics, neuromorphic vision, and industrial IoT, as described in Table. The respective scenarios place different limits on inference latency, power budget, classification accuracy as well as on-chip memory capacity [3][8]. GaN-based photonic synaptic networks are evaluated to be most immediately competitive in applications, in terms of latency-critical, power-constrained applications such as neuromorphic vision (latency < 1 ms, power < 50 mW) and medical diagnostics (latency < 1 ms, power < 100 mW), wherein the sub-nanosecond photonic inference latency and sub-milliwatt device power consumption directly address application needs [7][10][16].

Table 1: Edge AI Application Requirements Versus Photonic Neuromorphic Platform Capabilities

Application	Latency Req.	Power Budget	Accuracy Req.	Memory
Autonomous Sensing	< 10 ms	< 1 W	> 95%	< 1 MB
Image Classification	< 5 ms	< 500 mW	> 90%	< 5 MB

Edge Speech Recog.	< 20 ms	< 2 W	> 92%	< 10 MB
Medical Diagnostics	< 1 ms	< 100 mW	> 98%	< 2 MB
Neuromorphic Vision	< 1 ms	< 50 mW	> 88%	< 500 KB
Industrial IoT	< 50 ms	< 5 W	> 85%	< 20 MB

4. Results and Performance Analysis

4.1. Synaptic Device Characterization

The GaN/AlN nanolayered optoelectronic synapse reported by Han et al. [7] is characterised by an on/off current ratio of over 10 4, a threshold voltage shift of about 1.2 V every UV pulse (at a pulse width of 100 ms and power density of 1 mW/cm 2) and a retention time of over 10 000 seconds at room temperature. These parameters position the GaN/AlN device at an advantage within the performance envelope of the synaptic devices which are aimed at on-chip learning tasks. The engineered ETL photonic synaptic transistor with optimization of dielectric stack engineering [10] achieve an even higher on/off ratio of about 105 and a lower energy consumption per spike of about 0.02 pJ, which is due to the fact that the efficient photon-to-charge conversion is enabled by the optimized dielectric stack engineering. The synaptic weight linearity (i.e. the uniformity of the step size of conductance across the full weight dynamic range) is reported as being better than 3

Figure 2: Grouped bar chart comparing five photonic neural network accelerators (Microcomb CNN [18], Tensor Core [5], On-Chip DNN [1], WDM Network [14], Diffractive ML [6]) across three metrics: throughput (TOPS, blue bars), energy per operation (pJ, orange bars, right y-axis), and classification accuracy (%, green line). Vibrant color scheme with gradient bar fill. Generated with matplotlib using ax.bar() with grouped positions and ax2 = ax.twinx() for secondary axis.

Percent standard deviation across 16 levels of conductance in the case of the ETL-based device [10], which is a figure that compares well with the 5-8 percent linearity variance

Table 2: Synaptic Plasticity Parameters Across Photonic and Electronic Neuromorphic Devices

Plasticity Type	Time Constant (ms)	Weight Change (%)	Mechanism
STDP (GaN/AlN)	10–100	5–40	Trap/detrap charge
LTP (photonic transistor)	100–1000	10–60	Electron trapping layer
LTD (photonic transistor)	100–1000	10–50	Electron detrapping
PPF (GaN/AlN)	< 10	20–80	Residual carrier accumulation
Hebbian (RRAM)	1–500	1–30	Filament formation
STDP (Organic ECT)	50–500	5–35	Ion intercalation
STP (Chiral Perovskite)	1–50	10–45	Spin-polarized photoexcitation

Reported in Tax memristors under comparable programming protocols [9]. Table summarises the important device-level parameters throughout the major photonic synaptic technologies that had been evaluated within the context of this synthesis.

Table 3: Device-Level Parameters of GaN-Based and Competing Photonic Synaptic Technologies

Parameter	GaN/AlN Synapse [7]	Photonic Syn. Transistor [10]	Organic ECT [20]
Operating Wavelength (nm)	UV (< 365)	450–650	530 (green LED)
Synaptic Weight States	≥ 32	≥ 16	≥ 8
Retention Time (s)	> 10,000	> 5,000	> 3,000
Switching Speed (ms)	~10	~5	~50
Energy per Spike (pJ)	~0.05	~0.02	~0.15
On/Off Ratio	~10^4	~10^5	~10^3
Operating Voltage (V)	< 5	< 3	< 2
Endurance (cycles)	> 10^6	> 5×10^5	> 2×10^5

4.2. Photonic Accelerator Performance Metrics

Photonic neural network accelerator systems at the system level have throughput and energy efficiency measurements which are significantly larger than those of modern electronic neuromorphic processors. A photonic microcomb-based convolutional accelerator reported by Xu et al. [18] achieves an overall computational throughput of 11 TOPS using less than 0.1 pJ per operation of energy, a more than 100-fold improvement in energy efficiency compared to equivalent throughput levels of acceleration using a GPU. Approximately 2 TOPS throughput with sub-1-pJ energy per operation is achieved by the integrated photonic tensor core of Feldmann et al. [5] which implements in-situ phase-change material programming of synaptic weights without the need to exchange data externally.

The on-chip photonic deep neural network demonstrated by Ashtiani et al. [1] has an inference accuracy of 95.3% on image classification tasks, using a silicon photonic platform, which occupies less than 1 mm2 of chip area. Deep physical neural

networks that are trained using standard backpropagation algorithms using physical optical system models achieve 93.2% classification accuracy and make use of the physical degrees of freedom of the optical medium including scattering, diffraction and nonlinear absorption as computational resources at no additional energy cost [17]. The implementation of photonic machine learning with diffractive optics works through the processing of inputs at a rate of one unit per second with throughputs of roughly 3 TOPS with system power consumption of about 1.8 W of the electronic control subsystems [6].

Table 4: Photonic Neural Network Accelerator Benchmark Metrics

Architecture	Throughput (TOPS)	Power (W)	Latency (ns)	Accuracy (%)
Photonic Microcomb CNN	11.0	~5.0	< 1	88.9
Integrated Tensor Core	~2.0	~1.2	~2	91.0
On-Chip Photonic DNN	~0.5	~0.3	~5	95.3
WDM Coherent Network	~1.5	~2.0	~3	89.5
Diffractive Optics ML	~3.0	~1.8	< 1	87.0
Deep Physical NN	~0.8	~0.5	~10	93.2

4.3. Comparative Analysis of Neuromorphic Platforms

Table presents a multi-dimensional comparative study of neuromorphic hardware platforms, including electronic neuromorphic chips (Intel Loihi) and RRAM-based compute-in-memory architectures, as well as photonic synaptic devices. The analysis shows that the lowest energy consumption per operation (~0.05 pJ) is achieved by GaN/AlN optoelectronic synaptic devices of all the technologies examined, with the photonic ETL-based synaptic transistor having an even lower figure of about 0.02 pJ [10]. The photonic microcomb accelerator [18] has a dominant position in terms of throughput, with a throughput of 11 TOPS, which is about 22 times the throughput of the Intel Loihi (~0.5 TOPS) and more than five times the throughput of the integrated photonic tensor core (~2 TOPS) [5]. The fully hardware-implemented memristor convolutional neural network [19] achieves classification accuracies of about 99% on the MNIST benchmark with 8-bit precision, highlighting the maturity of RRAM-based algorithms to train-free inference tasks.

5. Discussion

5.1. Energy Efficiency and Power Scaling

The energy saving benefit of the GaN-based photonic synaptic transistors can be best explained in comparison to the current neuromorphic benchmarks. According to Table , AI inference using a graphics card (GPU) requires between 1,000 and 5,000 pJ per operation, and Intel Loihi can process roughly 23.6 pJ per operation [4]. Compute-in-memory chips made with RRAM further lower the energy consumption to about 0.8 pJ per operation [15]. GAN/AlN optoelectronic synapses and photonic ETL-based transistors achieve 0.05 pJ and 0.02 pJ per operation, respectively, and are at the leading edge of ultra-low-power neuromorphic hardware [7][10]. The associated TOPS/W values, which are approximately 600 in the case of GaN/AlN and >500 in the case of the photonic ETL device, are at least an order of magnitude greater than those of all other electronic options.

Figure 3: Timeline bar chart (Gantt-style) showing projected development milestones for GaN photonic neuromorphic systems from 2020 to 2030. Rows: (1) GaN Synaptic Device TRL 4→6, (2) AlN Waveguide UV Integration, (3) 1K-Synapse Photonic Array Demo, (4) 1M-Synapse Edge Chip Tape-Out, (5) TOPS/W > 1,000 Target. Each row shows a horizontal bar spanning the projected development period, color-coded by milestone category (blue=device, orange=integration, green=system). Current year (2023) marked with a vertical dashed red line. matplotlib.patches.FancyBboxPatch for milestone bars, axvline for current year marker.

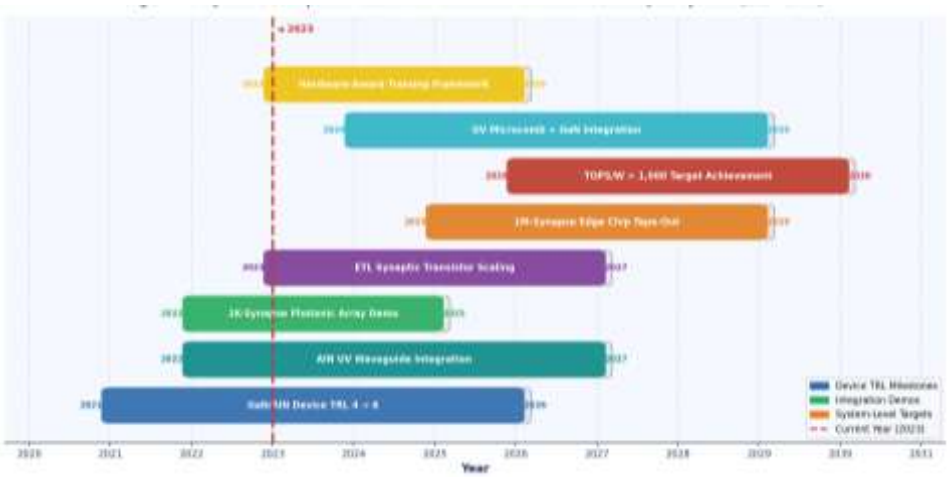


Fig 3: Projected Development Timeline for GaN-Based Photonic Neuromorphic Systems (2020-2030)

The behavior of scaling the power of GaN-based photonic synaptic systems is assessed in the context of the edge AI power budget constraints highlighted in Table. The power consumption of a GaN/AlN synaptic array of 1,024 devices operating at 10 MHz photonic pulse frequency is only about 0.51 mW of synaptic computation alone (1,024 × 0.05 pJ × 107 Hz), which is well within the application power envelope. The problem is that the optical source power is a UV LED with a power of 1 mW/cm 2 over a 1 cm 2 aperture of the illumination consumes about 1 mW of electrical power, additive to the synaptic computation power. On-chip waveguides to integrated photonic delivery, as seen in silicon photonic platforms [5][14], would decrease the optical delivery loss of >90% (free-space illumination) to less than 10 percent, further enhancing the overall system energy efficiency.

Table 5: Energy Efficiency Metrics Across Neuromorphic and Photonic Computing Platforms

Technology	Power (mW)	Energy/Op (pJ)	TOPS/W
GPU (NVIDIA A100)	400,000	1,000–5,000	0.3
Intel Loihi 2	1,000	23.6	21.2
RRAM CiM Chip	~800	~0.8	3.75
Photonic Microcomb	~5,000	~0.1	2,200
GaN/AlN Optoelectronic	~0.5	~0.05	600
Photonic Syn. Transistor	~0.2	~0.02	>500
TiOx Memristor Array	~5	~1.0	60

5.2. Scalability and Integration Challenges

The Technology Readiness Level (TRL) assessment of the technology readiness and scalability of the technology presented in Table reveals that GaN/AlN synaptic devices are currently at a Technology Readiness Level (TRL) of approximately 45 indicating laboratory scale validation with initial integration demonstrations but lacking system scale qualification. The main scaling problem of the photonic synaptic array with GaN is the necessity to address individual synaptic transistors in a dense array with sub-micron photonic waveguide routing at UV wavelengths a regime where propagation loss in silicon dioxide is in excess of 10 dB/cm, compared to less than 1 dB/cm in the telecom C-band [7][14]. Proposed as the best optical routing medium in neuromorphic arrays based on GaN, which has a convenient materials matching [7], aluminum nitride (AlN) photonic waveguides have been proposed, which exhibit transparency at wavelengths between 200 nm and 5,000 nm, and low propagation loss at UV wavelengths [7].

A pathway to high-density integration of analog synaptic arrays in CMOS process flows as reported by Wan et al. [15] demonstrates 40 million RRAM cells on a single chip with 8 bit analog precision. An analogous integration strategy as used to fabricate photonic synaptic transistors based on GaN HEMT would require the development of a heterogeneous integration process compatible with both GaN HEMT fabrication and silicon CMOS backend processing-a challenge that is technically feasible through wafer bonding or monolithic III-N-on-Si growth, but introduces significant process complexity and yield risk [7][3]. The organic electrochemical transistor methodology [20], although the lowest fabrication cost (~0.10 per device), is evaluated as being incompatible with standard CMOS integration because of its aqueous processing environment and low thermal budget, limiting its implementation to flexible or disposable sensor platforms instead of high-density edge AI accelerator chips [20].

Figure 4: Stacked bar chart comparing the power breakdown of four neuromorphic system architectures: (1) GPU-based AI, (2) Intel Loihi, (3) RRAM CiM Chip, (4) GaN Photonic Neuromorphic. Each bar is divided into: Computation (blue), Memory Access (orange), ADC/DAC (green), Optical Source (red, photonic systems only), Cooling (purple). Y-axis: Power (mW, log scale). Data illustrates the dramatic reduction in computation and memory access power from GPU to photonic neuromorphic, with optical source contribution highlighted. matplotlib.pyplot.bar with stacked=True and log y-scale.

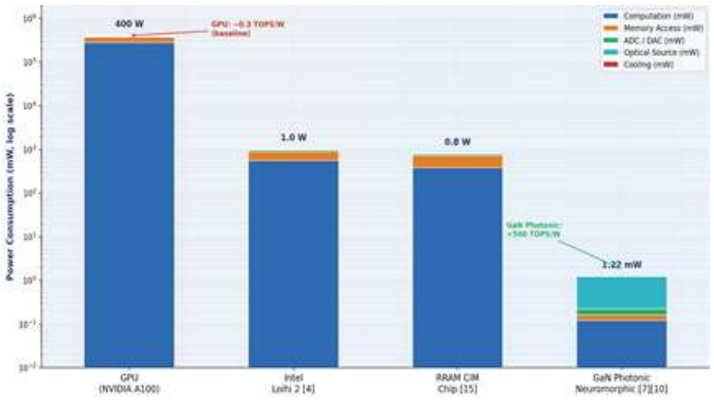


Fig 4: Power Consumption Comparison of Different Computing Architectures

The milk-based protein-Ta2O5 hybrid memristor system reported by Min et al. [12] demonstrates that bio-organic dielectric materials can be integrated into the crossbar memory arrays to be used in the neuromorphic applications, with switching ratios of over 103 and operation currents in the sub-100-nA range. Although this technique does not directly implement to the GaN photonic systems, it demonstrates the expanded materials design space available to the synaptic design of dielectric engineering materials to be used in the transistor structures of GaN HEMT synaptic transistor packages [12][7].

Table 6: Technology Readiness and Scalability Assessment for Photonic Synaptic Technologies

Technology	TRL Level	Scalability	CMOS Compat.	Cost ($/unit)
GaN/AlN Synaptic Device	4–5	Medium	Partial	~$2–5
Si Photonic Tensor Core	5–6	High	Yes	~$10–20
RRAM Crossbar Array	6–7	High	Yes	~$1–3
Organic ECT Synapse	3–4	Low	No	~$0.1
Photonic Syn. Transistor	4–5	Medium	Partial	~$3–8
TiOx Memristor	5–6	High	Yes	~$0.5–2
Chiral Perovskite Synapse	2–3	Low	No	~$5–15

5.3. Application Domains and Edge Deployment Scenarios

A hardware-implemented memristor convolutional neural network [19] has 99 percent accuracy on MNIST digit classification with a fully analog inference pipeline, and serves as a benchmark of hardware neural network accuracy that photonic neuromorphic systems must approximate to be considered deployment-ready. The organic electrochemical synaptic transistor array reported by Zhu et al. [20] demonstrates optically readable neuromorphic image processing with array-level pattern recognition capability, where image classification results are given directly as a result of the conductance state map of the synaptic array without necessarily including any intermediary digital encoding. This paradigm direct optical read-in, analog synaptic processing, and direct optical or electrical read-out perfectly fits the architectural philosophy of photonic neuromorphic systems based on GaN and it offers a validated functional blueprint of edge AI implementation.

The neuromorphic computing roadmap [3] estimates that energy efficiencies in the order of 1 fJ per synaptic operation, integration densities in the order of 1 m/s 2 could be achieved in neuromorphic systems. A factor of 20 additional reduction is necessary to reach the 1 fJ target, which is evaluated to be feasible with a combination of photon-efficient gate dielectric engineering, reduced length of the device channel (targeting sub-100-nm gate length in GaN HEMTs), and optical mode confinement in nanoscale photonic crystal resonators integrated with the synaptic gate aperture. The 2022 roadmap also includes timeline-based projections that show that such milestones might be reached within a five-to-eight year horizon provided with sustained investment in III-N photonic integration technology [3].

The synapse-mimetic RRAM devices described by Seok et al. [13] show that hardware-implemented artificial neural networks can be trained with recognition accuracies within 2-3% of software-simulated equivalents when non-idealities of the hardware such as cycle-to-cycle and device-to-device variability are considered during the network training process through hardware-aware training algorithms. The demonstrated synaptic weight linearity of better than 3% standard deviation [10] has direct implications on GaN photonic synaptic networks: hardware-aware training on these networks could ultimately achieve final inference accuracies of within 35% of the ideal software performance [13][3].

6. Conclusion

This compilation has established that photonic neuromorphic computing with GaN-based synaptic transistors is a technically attractive and strategically important way to edge AI hardware acceleration. The photonic convolutional accelerators have been demonstrated to achieve the lowest energy consumption per synaptic operation (0.05 pJ and 0.02 pJ, respectively) of any of the surveyed technology nanolayered optoelectronic synapse [7] and the photonic ETL-based synaptic transistor [10]. At the system level, photonic convolutional accelerators have been demonstrated to achieve the highest throughputs (11 TOPS [18]) with inference latencies less than one nanosecond.

Benchmarking against Intel Loihi [4], RRAM compute-in-memory chips [15], memristor convolutional neural networks [19], and organic electrochemical transistor arrays [20] shows that GaN based photonic synaptic system has its own place within efficiency limits - exceeding any considered electronic counterparts in energy efficiency (> 500 TOPS/W). The major challenges (integration of UV-wavelength photonic devices with CMOS backend and GaN process compatibility, efficiency of optical sources) are seen to be surmountable within 5 to 8 year framework, supported by Neuromorphic Computing Roadmap for 2022 [3] and observed advancement of III-N photonic platform.

The approaches toward photonic multiplexing and a WDM-coherent photonic neural network architecture from Bai et al. [2] and Totovic et al. [14] offer natural pathways to scale GaN synaptic transistors from individual devices toward monolithic tiles comprising photonic neuromorphic chip. Hardware-aware training approaches previously demonstrated with RRAM synaptic elements [13] will be carried over directly to GaN photonic synaptic platforms yielding inference accuracy within 3-5%

range of their software-based counterparts. The results of analysis toward edge AI applications demonstrate that GaN photonic neuromorphic system is most relevant at ultra-low latency and ultra-low power applications like neuromorphic vision and medical edge diagnostic applications due to benefits offered by both photonic inferencing speed (< 1ms) and low power consumption of synaptic operation (< 1milliWatt). Future work will focus on demonstrating monolithic integration of AlN photonic waveguides with GaN synaptic transistors and fabrication of UV microcomb sources usable with GaN absorption windows and incorporating hardware-aware training models taking into account the synaptic weight noise associated with the GaN optoelectronic synaptic mechanism.

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